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10/692,121	10/23/2003	Paul Edward Brucke	2003P52885US	2149

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,121	BRUCKE, PAUL EDWARD	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because it fails to describe the disclosure sufficiently within the range of 50 to 150 words. It is suggested that additional details of the invention be included in the abstract without exceeding 150 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-10, 12-14 and 16-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Jang (U.S. Pat. No. 6,219,292).

Regarding claims 1-7, Jang, for example in Figs. 3 and 4, discloses a method for activating a plurality of rows of a memory device, the method comprising: activating a

predefined number of the rows (determined by MRS) sequentially (see for example Fig. 4 which shows WL(b) being activated after WL(a)) in response to a single externally applied auto-refresh command (REF out of 20; see also Abstract which describes the invention as an auto-refresh operation; also, the auto-refresh command for Fig. 1 as applied to Fig. 3) issued by a memory controller (providing input signals to 20), wherein the predefined number is at least two of the plurality of rows (or less than all of the plurality of rows, or between two and four; for example, 2, 4 or 8; see column 5, lines 38-45); wherein activating the predefined number of the rows is done without an oscillator internal to the memory (see Fig. 3).

Regarding claims 8-10 and 12, Jang, for example in Figs. 3 and 4, discloses a method for activating rows of memory cells in a memory device comprising N rows of memory cells, the method comprising: issuing auto-refresh commands by a memory controller (providing input signals to 20) at a first frequency (the frequency at which the external auto-refresh commands are applied to 20 in Fig. 3), and in response to the auto-refresh commands, activating rows of the memory (determined by MRS) at a second frequency (the burst frequency) greater than the first frequency (since with one auto-refresh command, a burst of 2 to 8 rows are activated, before the next auto-refresh command, i.e., the burst frequency is greater than the frequency of the auto-refresh commands); wherein the first frequency is determined by the time needed to refresh a number of the rows at the second frequency (since the next auto-refresh command must wait until the burst refresh based on the previous auto-refresh is completed); and in response to each auto-refresh command, activating a predetermined number of rows of memory, the predetermined being greater than two (for example, 4 or 8; see column 5, lines 38-45).

Regarding claims 13, 14 and 16, Jang, in Figs. 3 and 4, discloses a method of activating rows of memory to be refreshed, comprising: initiating a first row activation (via the first enabled RASEN signal in response to REF from 20) of a first row in a memory array (for example, WL(a) in Fig. 4); in response to the row activation signal (the first enabled RASEN signal), invoking a first timing circuit (including 80) to issue a first refresh_end signal (related to PCG) signaling an end of the first row activation (by disabling RASEN via 70) after a period of time (associated with 80; see Fig. 4); in response to the refresh_end signal (since PCG disables RASEN and RAST), invoking a second timing circuit (including 60) to issue a refresh signal (IREF); and initiating a second row activation (via the second enabled RASEN signal in response to IREF) of a second row in the memory array (for example, WL(b) in Fig. 4) in response to the refresh signal (IREF, re-enabling RASEN via 70); disabling the second timer (by disabling REFEN after IREF is received at 40; see IREF and REFEN in Fig. 4; see also for example column 5, lines 64-67) after the refresh signal is issued (i.e., IREF is issued); and in response to the second row activation signal (the second enabled RASEN signal), invoking the first timing circuit (including 80) to issue a second refresh_end signal (the second PCG pulse from 80) signaling an end of the second row activation after the period of time (see PCG and RASEN in Fig. 4).

Regarding claims 17-26, Jang, for example in Figs. 3 and 4, discloses an on-chip refresh timing circuit for refreshing a memory device, comprising: a control circuit (including 70 and the NOR gate) comprising an auto-refresh command line (the output of 20) for receiving externally

initiated (or issued) auto-refresh commands (via 20); and a row activate output line (RASEN) for issuing row activate signals (the enabled RASEN signals), wherein the control circuit is configured to issue a first row activate signal (the first enabled RASEN signal in Fig. 4) in response to receiving an externally initiated refresh command (REF out of 20; see Fig. 4) on the command line; a first timer (including 80) coupled to the control circuit and configured to receive each of the row activate signals from the control circuit and issue a Refresh_End signal (related to PCG) a period of time, t1 (associated with 80; see also Fig. 4), after receiving each row activate signal from the control circuit; and a second timer (including 60) coupled to the control circuit and the first timer and configured to receive the Refresh_End signals from the first timer (via the disabled RASEN and RAST signals) and issue a refresh signal (IREF) a period of time, t2 (associated with 60), after receiving each Refresh_End signal (via disabling of RAST), wherein the refresh signal (IREF) causes the control circuit to issue at least a second row activate signal (the second enabled RASEN signal in Fig. 4) to the first timer; wherein the second timer is configured to issue (via IREF) a disabling signal (the output of 40) to disable the second timer (via the disabled REFEN; see also for example column 5, lines 64-67); wherein the disabling signal is the refresh signal (since IREF controls the ouput of 40 which disables the second timer); wherein the memory device is a memory array (10); wherein the second timing circuit comprises a latch (50) configured to output the refresh signal (IREF via REFEN) when the latch is set and a feedback line (for example, IREF line) on which the refresh signal is propagated back to the latch (via 40) to reset the latch and prevent a subsequent Refresh_End signal from causing issuance of a subsequent refresh signal (see for example column 5, lines 64-67); wherein the

control circuit, the first timer and the second timer are disposed on the memory device (see Fig. 3).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11, 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jang (U.S. Pat. No. 6,219,292) in view of Mullarkey (U.S. Pat. No. 6,208,577).

Jang discloses a memory device and a related method as in claims 8, 13 and 25 above, with the exception of issuing a self-refresh command to place the memory device in a self-refresh mode and disabling the second timer during self-refresh of the rows of memory.

Mullarkey discloses a memory wherein a self-refresh command is issued to place the memory device in a self-refresh mode during a low-power operation (see for example column 2, lines 56-67).

Since memories which include a self-refresh mode (a low-power, sleep mode) along with an auto-refresh mode were common and well-known in the art (as exemplified by Mullarkey), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate Jang's means for auto-refreshing into a memory that has both auto-refresh and self-refresh modes (such as that of Mullarkey), and disable during a self-refresh operation any circuit elements not needed by the self-refresh operation, including the second timer

associated with the auto-refresh mode, for the purpose of efficiently carrying out self-refresh or auto-refresh operations in such memory (see for example Jang, column 3, lines 2-5).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakaizumi et al. (U.S. Pat. No. 4,616,346) discloses an auto-refresh timer.

Parris (U.S. Pat. No. 5,430,680) discloses a self-timed burst refresh operation.

Biswas (U.S. Pat. No. 5,907,857) discloses burst refresh operations.

Schaefer et al. (U.S. Pat. No. 6,693,837) discloses a burst refresh.

Cowles, Timothy B. et al. (U.S. Pat. Appl. Pub. No. 2003/0076726) discloses an internal auto-refresh timer.

Aritomi, Kengo et al. (U.S. Pat. Appl. Pub. No. 2004/0196719) discloses a second refresh timer.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

3/29/05

jhh

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